Final Exam 2002

1) The circuit in Figure 1 uses ideal op-amps. Determine the output voltage, v_o, and the output current, i_o, with v_s = 1 V.

v_o = _____ i_o = _____

What direction is the output current, i_o, flowing?

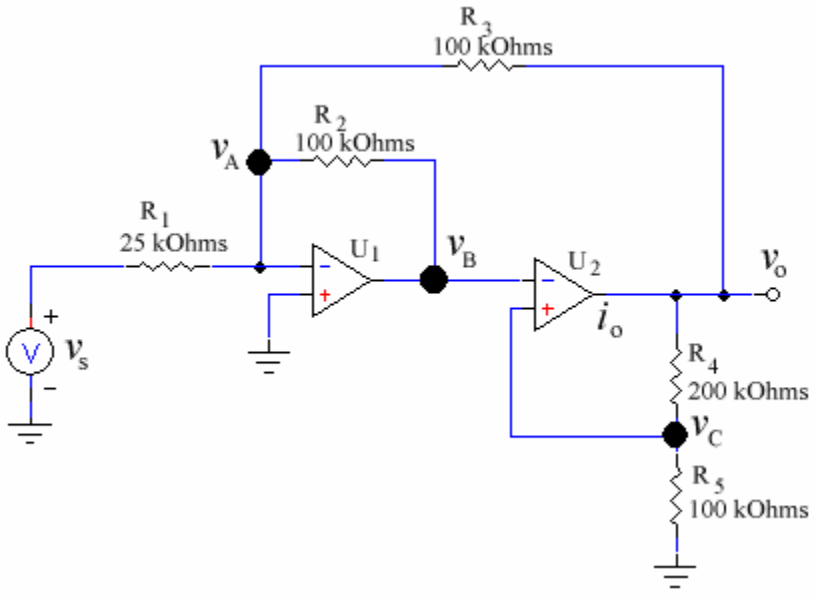


Figure 1

Final Exam 2002

2) The transistors, (Q_1 and Q_2) in Figure 2 are matched, and therefore have identical electrical characteristics.
Assume $\beta = 100$, $V_{BE} = -0.7$ V, $V_{CE(sat)} = -0.3$ V and $I_{CBO} = 20$ nA and it may also be assumed that $I_{B1} \approx I_{B2}$.

Compute the current through R_3 for the following supply voltages:

+Vsupply = +5 V **I** = _____

+Vsupply = +7 V **I** = _____

What is your conclusion?

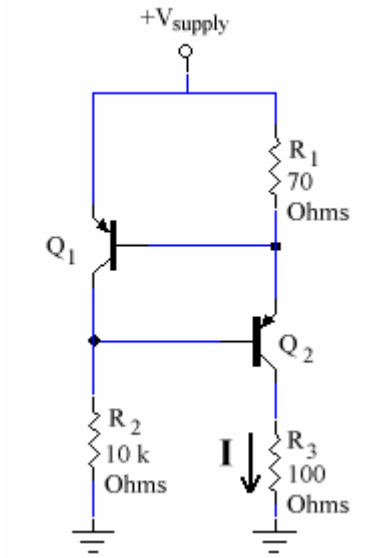


Figure 2

Final Exam 2002

3) For the two stage amplifier circuit shown in Figure 3, determine the input impedance, z_{in}, the overall voltage gain, A_V, and the output impedance, z_{out}. What would the output voltage be in volts peak to peak if the input generator had a source resistance of 1.216 kΩ and a level of 1 mV_{RMS} and the amplifier was driving an external 1.5 kΩ load?
Assume β = 100, V_{BE} = 0.7V, $V_{CE(sat)}$ = 0.3 V, I_{CBO} = 20 nA, and that the amplifiers are biased properly.

z_{in} = _____ z_{out} = _____ A_V = _____ v_{out} = _____ V_{P-P}

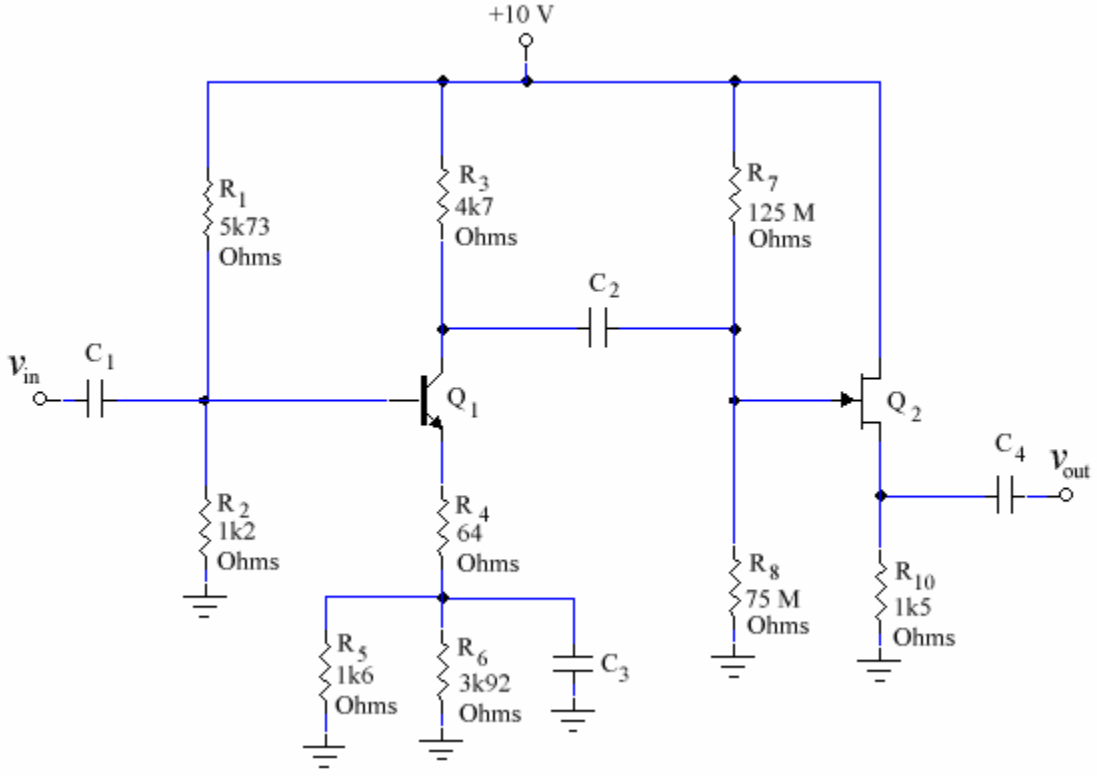
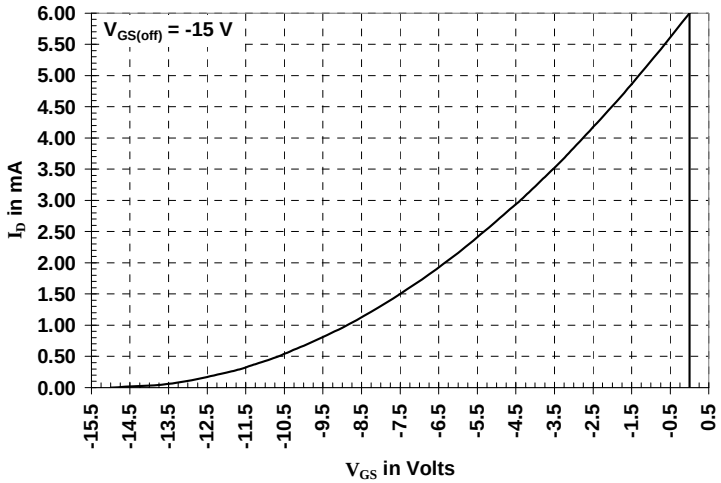


Figure 3



Final Exam 2002

4) For the circuit shown in Figure 4, calculate the value for R_4 that will place Q_1 in the middle of the V_{DS} load line. Assume $\beta = 100$, $V_{BE} = 0.7V$, $V_{CE(sat)} = 0.3$ V and $I_{CBO} = 20$ nA.

R_4 = _____

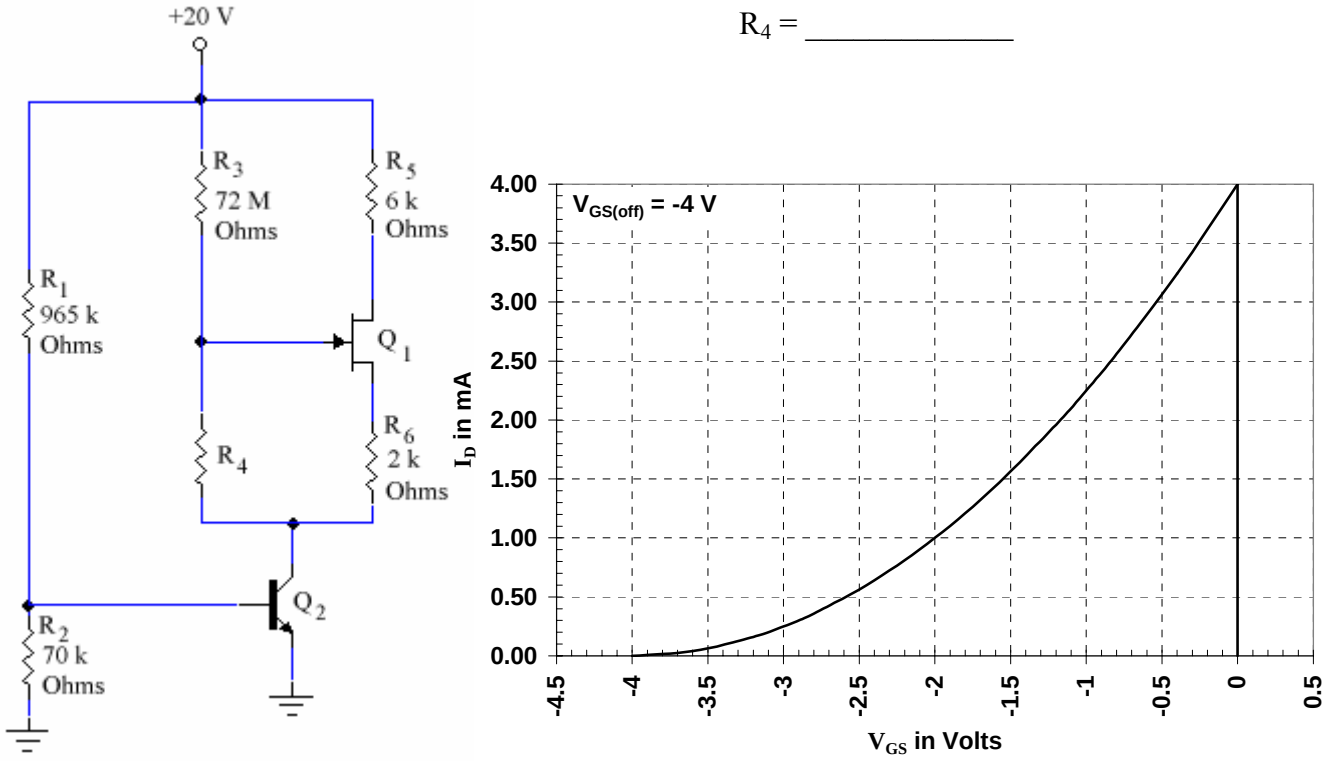


Figure 4

Final Exam 2002

5) The circuit shown in Figure 5 is a differential amplifier with a differential output. Determine the following using these assumptions:
Assume that $I_C = I_E$, $V_{BE} = 0.7$ V, and $V_{CE(sat)} = 0.3$ V for both BJT's but Q_1 has a $\beta_1 = 98$ and Q_2 has a $\beta_2 = 94$.

NOTE: If needed it may also be assumed that the equivalent resistance of Q_3 is 1.02 MΩ.

Determine:

I_C = _____ I_{bias} = _____ I_{offset} = _____

A_{cm} = _____ A_{dm} = _____ CMRR = _____dB

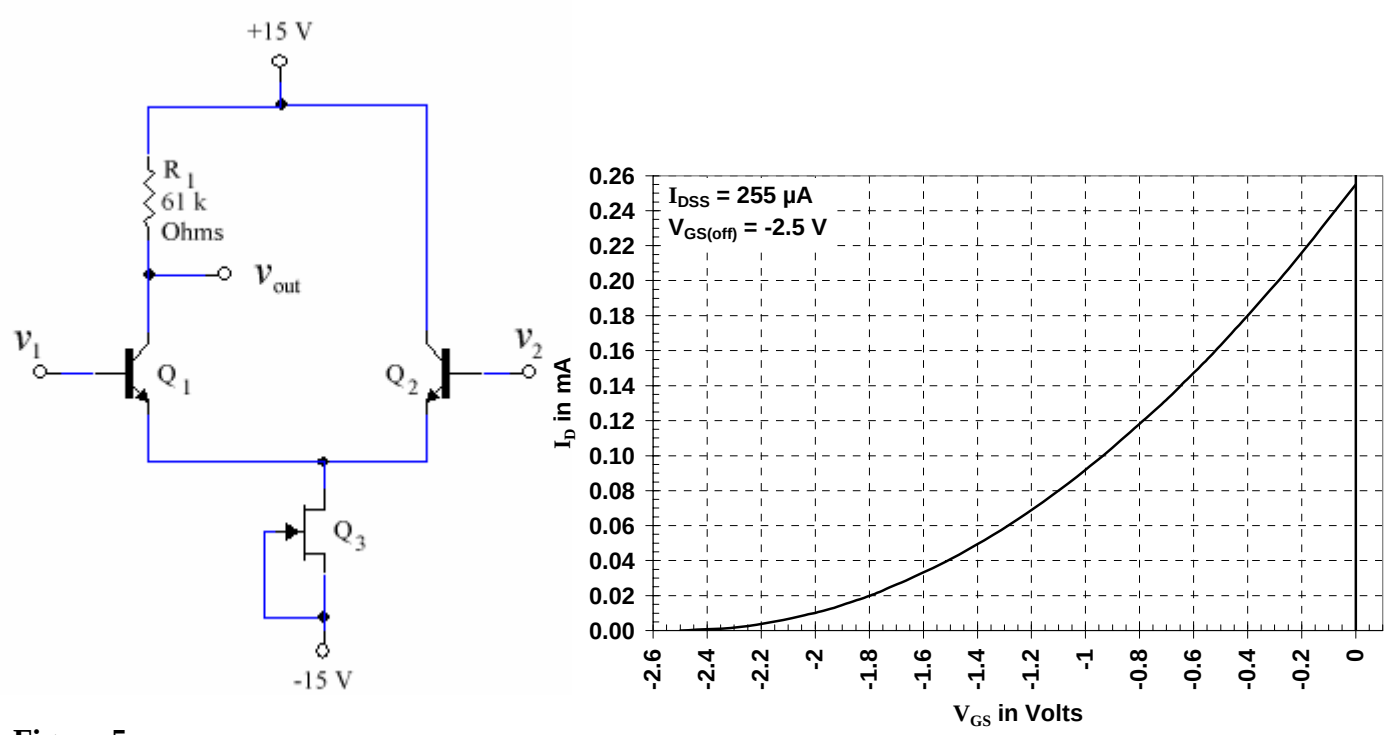


Figure 5

Bonus Question (1 Mark)
Which is the inverting and which is the non-inverting input for the diagram in Figure 5?

v_1 = _____

v_2 = _____